ATLAS IBL sensor qualification

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ATLAS IBL sensor qualification

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ABSTRACT: The upgrade of the ATLAS detector will undergo different phases towards high luminosity LHC. The first upgrade for the Pixel Detector will consist in the construction of a new pixel layer which will be installed during the first shutdown of the LHC machine (foreseen for 2013–14). The new detector, called Insertable B-Layer (IBL), will be inserted between the existing Pixel Detector and a new (smaller radius) beam-pipe at a radius of 3.2 cm. The IBL will require the development of several new technologies to cope with increase of radiation or pixel occupancy and also to improve the physics performance which will be achieved by reduction of the pixel size and of the material budget. Two different promising Silicon sensor technologies (Planar n-in-n and 3D) are currently under investigation for the Pixel Detector.

An overview of the sensor technologies qualification with particular emphasis on irradiation and beam tests will be presented.

KEYWORDS: Solid state detectors; Radiation-hard detectors; Large detector systems for particle and astroparticle physics; Particle tracking detectors (Solid-state detectors)

[1] On behalf of the ATLAS IBL collaboration.

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1 Introduction

The ATLAS [1] Pixel Detector [2] is the innermost part of the ATLAS experiment and therefore the one suffering the most from the severe radiation environment induced by the LHC in ATLAS. Due to the expected limited lifetime of the B-layer sensors (the layer closest to the beam pipe) its performance will decrease well before the main tracker upgrade around 2020. To ensure the excellent tracking and vertexing performance of the Pixel Detector, which is especially necessary in the high pile-up environment of the LHC Phase-I upgrade, it was decided to add a fourth layer between the current B-layer and a new beampipe. Installation of this Insertable B-Layer (IBL) [3] is foreseen for the long shutdown in 2013-2014.

Due to the increased radiation levels at the IBL radius of 3.2 cm, extremely radiation hard technologies are required for the sensors and readout chips. Until replacement of the IBL, the projected radiation doses, including safety factors, are 250 Mrad of Total Ionising Dose (TID) and 5×10^{15} $n_{eq}cm^2$ of Non-Ionising Energy Loss (NIEL).

Two different pixel sensor technologies are envisaged for the IBL. One option is developed by the ATLAS Planar Pixel Sensor (PPS) Collaboration and is based on classical silicon sensors where the electrodes are implanted on the surface of the wafer. The other option is developed by the ATLAS 3D Collaboration. 3D silicon technology is an innovative combination of VSLI and MEMS (Micro-Electro-Mechanical-Systems) where electrodes are fabricated inside the silicon bulk.

2 Sensor technologies

Sensor development for IBL is driven by the radiation levels as well as the available space. The IBL modules will not have any overlap in z direction, yet to minimize inefficiencies it is required, that inactive regions at the sensor edges should be smaller than 450 μm. The bias voltage is limited to a maximum value of 1000 V by the insulation of the cables.

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2.1 Planar sensors

The planar sensor design uses n-in-n sensors, processed on diffusion oxygenated float-zone (DOFZ) silicon wafers [4]. In order to meet the requirement for the maximum inactive area, a slim edge sensor was designed, that reduces the inactive edge by shifting the guardrings partially into the sensitive region opposite the outermost pixels and elongating these pixels from the ususal 250 μm to 500 μm in z direction.

The sensor thickness of 200 μm is slightly less than the current ATLAS Pixel sensors. After irradiation, this promises higher charges with respect to thicker sensors at the same bias voltage as the higher charge carrier velocity reduces the trapping probability.

2.2 3D sensors

The original design of 3D sensor was proposed in 1997 [5]. Instead of being implanted on the surface of the wafer, electrodes are processed through the thickness of the wafer. This has the main advantage of considerably reducing the distance between the electrodes. The inter-electrode spacing for the 3D IBL sensor is 67 μm. The short inter-electrode distance ensures low depletion voltage and therefore low dissipated power, fast charge collection and smaller trapping probability.

In the IBL sensor design, the electrodes are processed from both sides of the wafer and penetrate the full thickness. A guard fence design allows to reduce the inactive area at the sensor edge significantly.

3 Irradiation and beam test campaigns

In order to qualify the sensor technologies for use in IBL, an extensive program of irradiations and beam tests was conducted. A number of samples were irradiated to the IBL target fluence of 5×10^{15} n_{eq}/cm^2. Irradiations were carried out using thermal neutrons in the TRIGA reactor at Jozef Stefan Institute, Ljubljana, and 26 MeV protons at Karlsruhe Institute for technology, with the samples unpowered. In both cases, the irradiation to the IBL target fluence is completed within few minutes. The samples are not cooled during this short period. Due to the low energy in the proton irradiations, the total ionizing dose (TID) the assemblies were subjected to, are on the order of 750 Mrad, which is about three times higher than the IBL lifetime dose. This led to a small but significant number of failing readout cells in the FE-I4 chip. These pixels were excluded from further analysis.

Samples before and after irradiation were tested in various beam test campaigns using 4 GeV positrons at the DESYII synchrotron at DESY, Hamburg, as well as 180 GeV pions at CERN SPS. The high resolution EUDET telescope [7] was used for tracking. Some results from the SPS test-beam at CERN are presented here.

3.1 Hit efficiency

The hit efficiency for each device under test (DUT) is estimated using tracks extrapolated from the telescope to the DUT, where matching hits are checked for. For each track, one or more hits in other DUTs are requested to suppress fake tracks due to the long integration time of the telescope.

The measured hit efficiencies for unirradiated planar and 3D devices are 99.9% and 99.6% respectively, at normal incidence. The slightly lower efficiency of the 3D samples has been shown

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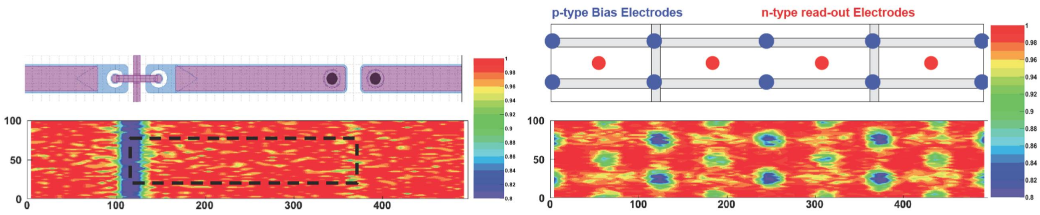

Figure 1. Cell efficiency maps for a planar sample, irradiated to 6×10^{15} n^{eq}/cm^2 (left) and a 3D sample, irradiated to 5×10^{15} n^{eq}/cm^2 (right). Two cells are shown: a central cell, and two half cells in the horizontal and vertical directions. The dimensions are given in μm. The upper sketch shows the corresponding lithography. The data for the left plot was taken at 15° track incidence, for the right plot data was taken at normal incidence.

Table 1. Hit efficiencies measured in the testbeam at CERN.

Sample ID	Type	Fluence $[n_{eq}/cm^2]$	Hit Efficiency [%]
SCC45	planar	0	99.9
SCC55	3D CNM	0	99.6
SCC61	planar	6E15 protons	96.9
LUB2	planar	4E15 neutrons	99.0
SCC34	3D CNM	5E15 protons	97.5
SCC97	3D CNM	6E15 protons	97.4
SCC82	3D CNM	5E15 neutrons	89.4
SCC87	3D FBK	5E15 protons	95.3
SCC90	3D FBK	2E15 protons	99.8

to originate from tracks passing through the electrodes [6], and increases to 99.9% for tracks inclined by 15°.

An overview of the hit efficiencies measured for the different devices can be found in table 1. The low efficiency of sample SCC82 is due to underdepletion.

Figure 1 shows the efficiency maps in the pixel cells, where all cells have been added up. The left plot shows a planar sample (SCC61) at a track incidence angle of 15°, the right plot shows a 3D sample (SCC34) at normal track incidence. Two cells are shown in the respective plots: the central cell and two half cells in both the horizontal and vertical directions. The corresponding lithography sketch is also shown. The bias grid and dots, and solder bumps are seen on the left and right of the sketch, respectively. For the planar sample, efficiency loss is observed at the edge of the cells, mainly due to charge sharing. More efficiency loss occurs on the bias dots side. This is explained as some charge is trapped and lost in the bias grids and dots. For the 3D sample, efficiency loss is observed in the regions of the electrodes. These do not penetrate the whole thickness of the bulk, which is why the efficiency does not drop to zero in this region.

3.2 Edge efficiency

To measure the width of the inactive edge of the sensors, hit efficiency was measured as a function of the distance from the sensor edge. Figure 2 shows the exemplary result of the measurement for an unirradiated 3D sample.

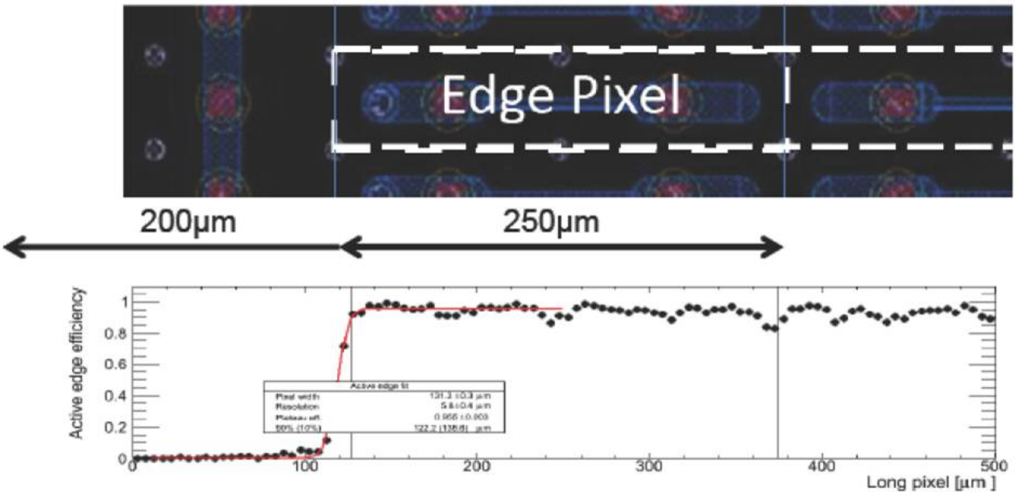

Figure 2. Hit efficiency as a function of the distance from the physical sensor edge for an unirradiated 3D sample. The upper sketch shows the corresponding lithography.

For planar samples an effective inactive width of 215 μm was measured, for 3D samples the inactive width is 170 μm. Both technologies clearly exceed the IBL requirement.

3.3 Charge collection

One of the main areas of interest during the beam tests was the collected charge after irradiation. The FE-I4 provides charge measurement through a time-over-threshold (TOT) mechanism with a resolution of 4 bit.

Due to some issues in the calibration of the mechanism, conversion of TOT into charge is not possible for the data collected in the CERN testbeam. However, based on the high hit efficiency of the samples, it is safe to assume that the charge-to-threshold ratio is large enough after irradiation to operate both types of sensors reliably until the end of the IBL lifetime.

4 Conclusion

ATLAS currently develops and constructs a new Pixel Detector for the first upgrade of its tracking system: The ATLAS Insertable B-Layer Pixel Detector (IBL). The new layer will be inserted between the innermost layer of the current Pixel Detector and a new beam pipe. A new generation of pixel FE-chip has been developed and tested extensively with planar and 3D silicon pixel sensors for the IBL. An extensive qualification program for the sensors for the ATLAS IBL Upgrade was conducted successfully, including irradiation and beam test campaigns.

Production of sensors, chips, modules and staves has started. The construction and installation is expected to be completed in the LHC shutdown of 2013.

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