Recent achievements of the ATLAS upgrade Planar Pixel Sensors R&D Project

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ABSTRACT: After the foreseen upgrade of the LHC towards the HL-LHC, coming along with higher beam energies and increased peak luminosities, the experiments have to upgrade their detector systems to cope with the expected higher occupancies and radiation damages. In case of the ATLAS experiment a new Inner Tracker will be installed in this context. The ATLAS Planar Pixel Sensor R&D Project (PPS) is investigating the possibilities to cope with these new requirements, using planar pixel silicon sensors, working in a collaboration of 17 institutions and more than 80 scientists. Since the new Inner Tracker is supposed to have an active area on the order of $8\,m^2$ on the one side and has to withstand extreme irradiation on the other side, the PPS community is working on several approaches to reduce production costs, while increasing the radiation tolerance of the sensors. Another challenge is to produce sensors in such large quantities. During the production of the Insertable b-Layer (IBL) modules, the PPS community has proven to be able to produce a large scale production of planar silicon sensors with a high yield. For cost reduction reasons, it is desirable to produce larger sensors. There the PPS community is working on so called quad- and hex-modules, which have a size of four, respectively six FE-I4 readout chips. To cope with smaller radii and strict material budget requirements for the new pixel layers, developments towards sensors with small inactive areas are in the focus of research. Different production techniques, which even allow the production of sensors with active edges, have been investigated and the designs were qualified using lab and testbeam measurements. The short distance between the new innermost pixel layers and the interaction point, combined with the increase in luminosity, requires designs which are more radiation tolerant. Since charge collection on the one hand decreases with irradiation and on the other hand is not uniform within the pixel cells, design modifications of the pixel

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implantations are under investigation. The latest achievements of these topics are presented in this paper.

Contents

1   Planned ATLAS upgrades

The current long shutdown of the LHC and its experiments is one out of three scheduled downtime phases for upgrades on the accelerator and experiments' components. The upgrades are aiming to extend the physics reach of the LHC measurement programme. Following that aim, not only the beam energy will be increased to the design value of 14 TeV, but also the peak luminosity will be ramped up to possibly $(5-8) \cdot 10^{34} \, \mathrm{cm}^{-2}\mathrm{s}^{-1}$ [1]. This stepwise increase in luminosity requires different planned upgrades of the ATLAS detector. In this paper the focus is exclusively on the upgrades of the innermost detector system, the pixel detector. The present ATLAS pixel detector [2] is realized in a three-layer cylindrical setup at radii of 50.5 mm, 88.5 mm and 122.5 mm in addition to three disc end-cap layers on each side. In total, this adds up to 1744 pixel modules, each consisting of a 250 μm thick n-in-n planar silicon sensor, connected to 16 readout chips of the FE-I3 generation. The current pixel modules are rated and tested up to a fluence of $10^{15} \frac{n_{eq}}{\mathrm{cm}^2}$.

The first big upgrade project of the pixel detector is ongoing during the current first long shutdown phase (called "phase 0"), which started beginning of 2013 and lasts until end of 2014. After the shutdown, on the accelerator side there will be a significant increase in the provided luminosity. To cope with this increased luminosity a new fourth detector layer will be installed inside the current pixel detector at a radius of 32 mm, the so called Insertable b-Layer (IBL) [3]. The small radius, together with space constraints, do not allow overlapping sensors in z-direction anymore, therefore the active area of the new sensors had to be increased. Because of the position close to the interaction point, the IBL devices have to be very radiation tolerant and have to cope with a very high hit occupancy. Consequently, new sensor materials and designs were investigated. On the readout side a new readout chip, called FE-I4 [4], was developed. Each FE-I4 chip hosts 26880 pixel cells, which means roughly an increase by a factor of ten compared to the FE-I3 chip. The pixel size was shrunk down to 50 μm × 250 μm, while the radiation tolerance was rated and tested up to the expected lifetime fluence (plus safety factors) of $5 \cdot 10^{15} \frac{n_{eq}}{\mathrm{cm}^2}$ and even beyond. This upgraded pixel system is expected to provide sufficient tracking even after the next scheduled long shutdown ("phase I"), which is planned for the year 2018.

The subsequent long shutdown, called "phase II", is foreseen for the years 2022 and 2023. During the phase II shutdown a complete replacement of the ATLAS inner tracker is planned. This leads to different new tasks. On the one hand large scale production techniques have to be pursued to be able to cover an extended pixel system area, while reducing costs. On the other hand higher expected occupancies make higher granularities and a radiation tolerance of up to $2 \cdot 10^{16} \frac{n_{eq}}{\mathrm{cm}^2}$ necessary, as well as reduced geometrical inefficiencies due to material budget restrictions.

2 Activities and achievements towards the phase II upgrade

As previously explained, the planned phase II upgrade implies a number of new challenges for the pixel system. Within the Planar Pixel Sensor R&D Project solutions for these new tasks are being investigated and the most recent developments on the different tasks are reported in this paper.

2.1 IBL production — medium scale production

During production of the ATLAS IBL modules, the PPS community has proven its capability of driving a medium scale production with high yield. In total, 150 wafers, containing 600 IBL single/double chip sensors, were produced and were bump bonded to FE-I4 readout chips. Each sensor has a design thickness of $200\,\mu\mathrm{m}$ and a total size of $41300\,\mu\mathrm{m} \times 18600\,\mu\mathrm{m}$, covering two FE-I4 readout chips. All planar IBL sensors were produced at CiS[1] and bump bonded at IZM.[2] After each production step all devices passed different quality checks [5]. In summary, a production yield of about 90.6% could be achieved, taking into account the good sensors after production, which were handed over to under bump metallization and dicing.

Since the ATLAS pixel system will have a significant growth in area within the phase II upgrade, a main issue is the possibility to produce large amounts of sensors with a high yield at low cost. In total the pixel system might grow up to an unprecedented sensor area of $8.2\,\mathrm{m}^2$, corresponding to about $638 \cdot 10^6$ channels [6]. The phase II baseline layout especially leads to a higher coverage in eta and a larger pixel barrel radius, resulting in a much larger sensor area, compared to the current ATLAS pixel system.

2.2 Large sensors — quad and hex modules

Beside a high production yield, another important point of bringing production costs down is to produce sensors with low processing expenditures. Since one of the main cost drivers in the current pixel sensor production is the bump bonding, where the price depends on the quantity and not on the size of devices to be treated, it is desirable to have larger sensors for future large scale developments. Already for the IBL production, so called double-chip sensors are used, where each sensor has the size of two FE-I4 chips. As a first approach to larger sensors, new wafers were produced by the KEK group,[3] the University of Liverpool[4] and the MPP group[5] together with the University of Göttingen, which include quad or hex sensors. These sensors were produced by CiS, HPK and Micron. Wafer designs are shown in figure 1.

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[1]CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt (Germany), www.cismst.org.

[2]Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin (Germany), www.izm.fraunhofer.de.

[3]www.kek.jp.

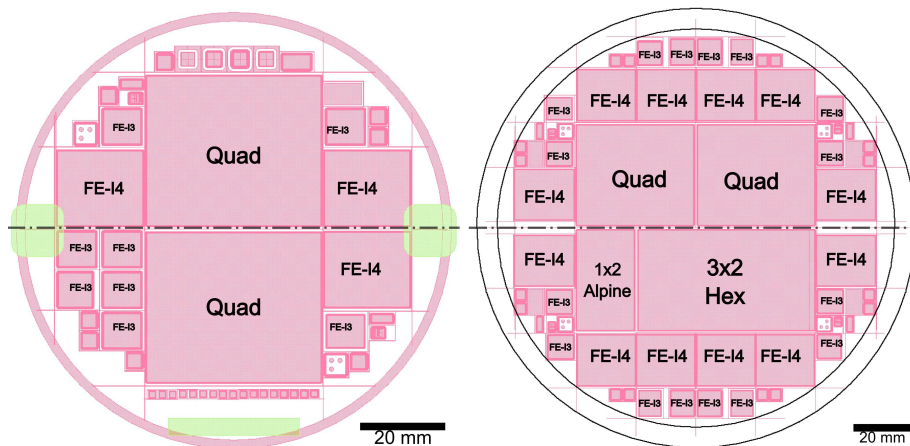[4]www.liv.ac.uk/particle-physics.

[5]www.mpp.mpg.de.

Figure 1. Left: wafer layout for 4" wafer, including sensors of FE-I3 size, FE-I4 size, as well as sensor of four times FE-I4 size ("quad"). Right: wafer layout for new 6" wafer, containing two sensors, each with a size of four FE-I4 chips and one sensor with a size of six FE-I4 chips ("hex").

The produced quad modules were characterized in laboratory, as well as beam tests at DESY. Results of the first laboratory tests of a fully operated quad module can be seen in figure 2. The histogram shows on the left the threshold distribution of a quad module, which is tuned to a target of $3000\,e^-$. On the right the corresponding noise distribution after threshold tuning is shown. Most pixels show the expected noise value of around $160\,e^-$, except the extended inter-chip pixels between chip 0 and 1, respectively chip 2 and 3. The higher noise value of these longer pixels can be seen as a shoulder in the central plot, as well as in the scatter plot, represented by the two peaks (due to the channel-wise counting). The measurements were performed using an extended version of the USBpix test system [8]. In figure 3 a picture of the quad module is shown. Larger numbers of quad and hex modules will be produced in the near future to investigate the operability and yield of large scale modules.

2.3   Slim/active edge approaches

Planar silicon sensors, which are currently being used in high energy physics experiments, are equipped with a non-active edge region (see figure 4). This region was implemented in the design to bring down the high voltage potential step by step from the HV pad towards the edge. On top of that, a safety margin between the last guard ring and the cutting edge was used. Since the design requirements of phase II include a reduction in the material budget, while keeping the geometrical efficiency as high as possible, different approaches towards reducing the edge width and designing active edge [9] regions, are followed. While typically the width of the edge region was in the order of $500\,\mu m$ to $1000\,\mu m$, now sensors with edge widths on the order of $100\,\mu m$ or less can be produced, which are operable in a comparable parameter range, using new technologies. One of the technologies used to achieve these so called "slim edge" sensors, is the *scribe-cleave-passivate (SCP)* technique. While conventional silicon sensors are separated by a saw or laser, both leading to the formation of defects along the edge with augmented conductivity, the SCP avoids this effect [10]. The aim of this technique is to have a resistive edge, such that the potential gradient
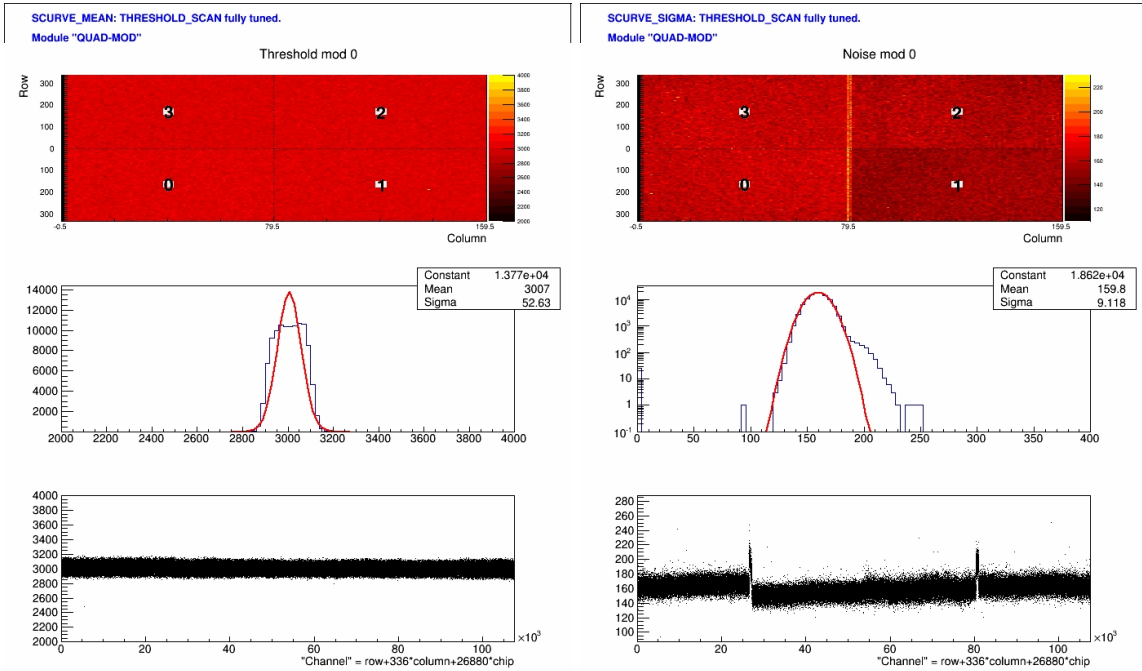
Figure 2. Left: threshold distribution of a full quad module after tuning to a target of $3000\,e^-$. Right: noise distribution of a quad module after threshold tuning. Most pixels show the expected noise value of around $160\,e^-$, except the extended inter-chip pixels between chip 0 and 1, respectively chip 2 and 3. These pixels correspond to the two peaks (due to the channel-wise counting) in the scatter plot.
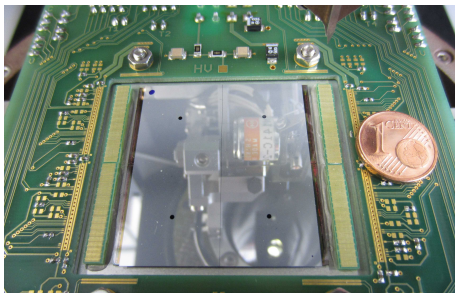

Figure 3. Quad module before wire-bonding with a coin for size comparison. The blue point in the upper left corner indicates the position of FE chip 0.
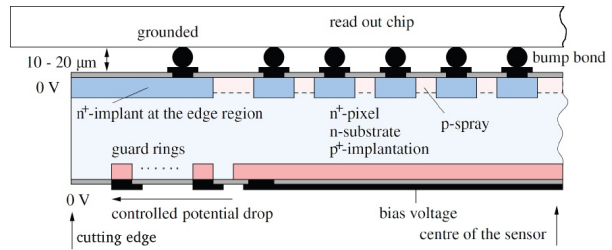

Figure 4. Schematic layout of the current ATLAS pixel sensor, showing the inactive edge region including guard rings and a safety margin on the left side [7].

can evolve along the edge surface. A key feature of the SCP technique is that it can be used as a post-processing step. In detail, the following processing steps are required:

First the sensor surface is scribed along the lattice orientation on one side of the sensor. For this first step, diamond scribing, laser scribing and surface trench-etching have been tested successfully. Afterwards the device is cleaved by mechanical stress, where manual cleaving using tweezers and industrial machine based cleaving have both been shown to work. After cleaving, a sidewall damage removal using XeF_2 can be done optionally, which leads to better results after passivation. XeF_2 can even be used for the scribing process. A comparison between laser scribed and XeF_2
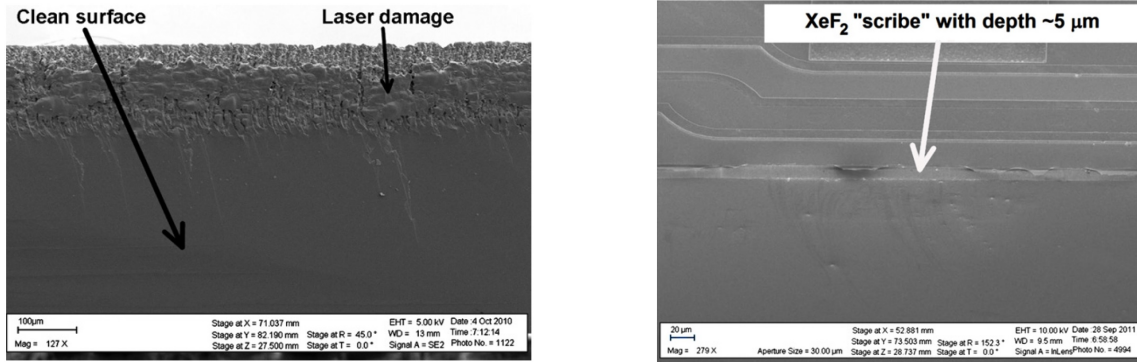
Figure 5. Left: image of an SCP processed sensor sidewall, where at the top a layer of defects is visible due to scribing, while the cleaving part below has a low density of defects. Right: image of a sensor edge, which was scribed using XeF$_2$, resulting in a low number of defects along the whole edge.
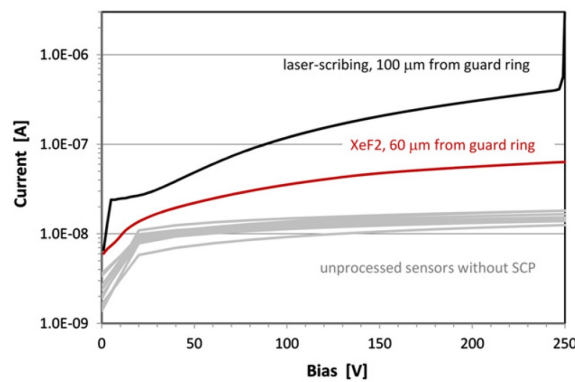

Figure 6. Comparison of the sensor leakage current after applying the SCP technique, using laser scribing (black) or XeF$_2$ scribing (red). The XeF$_2$ based scribing leads to much lower leakage currents, which corresponds to a smaller number of defects along the sensor edge.

scribed devices can be seen in figure 5. The concentration of defects along the edge can also be indirectly measured in terms of leakage current vs bias voltage. Also in that measurement XeF$_2$ scribed devices show very good results, as it is shown in figure 6.

Finally, the edges are passivated, using a dielectric. The passivation material depends on the sensor type. If the sensors have a p-type bulk, which require negative charges for passivation, then the edges are processed using Al$_2$O$_3$, while n-type devices are passivated using SiO$_2$ or Si$_3$N$_4$. Another approach towards slim or even active edges is the *deep reactive ion etching (DRIE)*. In this technique a vertical trench is etched through the entire wafer thickness, resulting in a cut which is almost free of damages, as well as a heavily doped trench. This means that the ohmic contact of the sensor backside extends throughout the edge, thus the depletion region grows towards the edge, while the increase in leakage current is relatively small. First n-in-p pixel sensors using the DRIE technique have been produced at FBK.[6] During production, a high-dose boron implant is performed on the sensor backside. For proper insulation of the n-type pixels on the front side p-spray and p-stop techniques are applied. For further details, see [11]. After the trench etching

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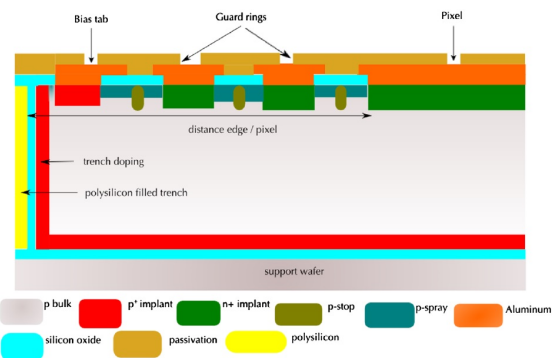[6]Fondazione Bruno Kessler, Trento (Italy), www.fbk.eu.

Figure 7. Schematic of an active pixel edge design after DRIE processing. This design includes guard rings, bias tabs, the doped trench and a support wafer, which is required for the process.
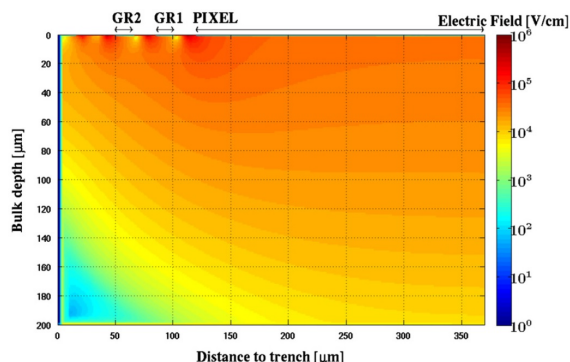
Figure 8. TCAD simulation of the electrical field distribution for an irradiated ($10^{15} \frac{n_{eq}}{cm^2}$) active edge device with two guard rings and an outer pixel to edge distance of 100 μm. The depletion voltage is 400 V.

process, the device walls are boron doped using a diffusion furnace, resulting in a continuous ohmic contact along the backside, continuing throughout the edge, as it can be seen in figure 7. Finally the trenches are oxidated, filled with poly silicon and undergo some standardized post-processing steps. Since the trench is etched through the whole device thickness, a support wafer is necessary. Currently several approaches how to safely remove the support wafer after the process are under investigation.

To achieve information on the shape of the electrical field distribution of different active edge designs, TCAD simulations have been performed [12]. In figure 8, the shape of the electrical field in a device, irradiated up to $10^{15} \frac{n_{eq}}{cm^2}$, biased with 400 V, is simulated. This design has a distance of 100 μm between the sensor edge and the outermost pixel and two guard rings. It can be clearly seen that the depletion zone reaches throughout the whole sensor bulk, with a small undepleted zone in the lower left corner. Since most of the bulk material is depleted and especially the depletion is on the pixel side, charge collection is possible up to the sensor edge. Information about further DRIE developments at other institutes can be found in [13].

2.4 Modifications to pixel implantations on n-in-n pixel sensors

Investigations of highly irradiated planar sensors show more charge than predicted with trapping models [14]. To study such possible charge amplification effects on planar n-in-n pixel sensors, a prototype sensor test structure was produced which fits to FE-I4 readout chips. Figure 9 shows pixel cells which try to force field strength maxima by modifying the shape of the pixel implantations. In the standard pixel layout V0, the electric field lines run homogeneously to the large, single electrode. In the other geometries, they are bent and thus focused in smaller regions due to the divided or narrowed implantations. The pixel implant variations especially include stepwise increasing subdivisions to clarify if this approach can contribute to cause higher electric fields and to enhance charge amplifications effects in highly irradiated n-in-n pixel sensors. More details of the layout can be found in [5]. In order to have a direct comparison between the performance of the different pixel versions, all of them are placed on one FE-I4 sized single chip sensor. Always 10 columns of the sensor feature the same version of pixel implantation shape. First lab tests with
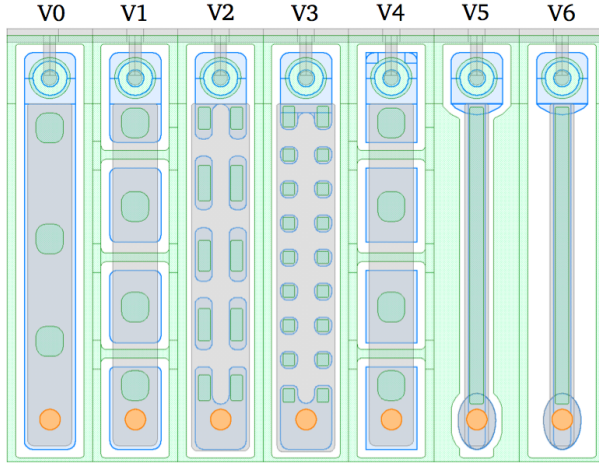
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Figure 9. Sketch of six different pixel implantations. The variants differ in the number of edges which are supposed to provoke high field strength as well as in the thickness [5].
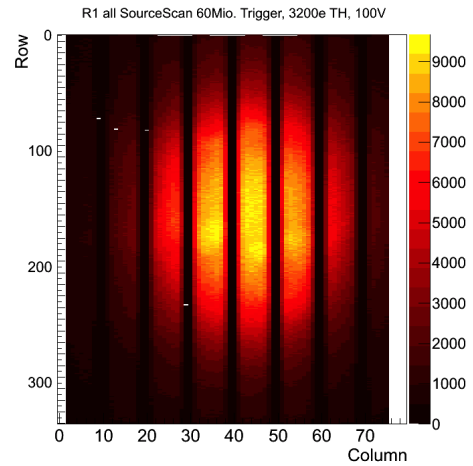

Figure 10. Beamspot taken with a FE-I4 sized single chip assembly employing different pixel implants on the n-in-n pixel sensor. See text for details.

non-irradiated structures, flip-chipped to FE-I4 readout chips, showed the possible operation of such R&D pixel sensors. Figure 10 shows a consistent beam spot in the modified pixel cells which has been derived from impinging beta particles, emerging from a Sr-90 source, traversing the sensor assembly. Events are triggered by a scintillator which was mounted opposite to the source, beneath the sensor assembly. First data derived in testbeam environments using high energy electrons are under investigation and further studies with irradiated assemblies of this kind are foreseen.

3   Conclusion & outlook

The planar pixel sensors approach is an established and well understood technology, which has shown its reliability and performance already in the existing trackers of the ATLAS and CMS experiments. Looking towards the harsh requirements of the phase II upgrade, the PPS community has shown that different approaches towards higher geometrical efficiencies, producing active edge sensors, cost effective large sensors and also large scale productions with high yields are possible. New pixel implantation designs have been realized to investigate possible charge amplification effects on highly irradiated sensors. Finally, developments towards reducing in-pixel efficiency inhomogeneities by changing the bias grid design and pixel isolations, are ongoing [15]. In summary, the PPS community shows promising approaches to fulfil the expected phase II requirements.

Acknowledgments

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